

M. MANSOUR DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
AMERICAN UNIVERSITY OF BEIRUT
FALL TERM 2005-2006
MIDTERM II

EECE320 - DIGITAL SYTEMS DESIGN

December 19, 2005

NAME: _____

ID: _____

COURSE SECTION: SECTIONS 2 & 3 (PROF. MANSOUR)

INSTRUCTIONS:

- **THE EXAM IS CLOSED BOOK/CLOSED NOTES. THE DURATION IS 1.5 HOURS.**
- **CALCULATORS ARE NOT ALLOWED.**
- **WRITE YOUR NAME AND ID NUMBER IN THE SPACE PROVIDED ABOVE.**
- **INDICATE THE SECTION YOU ARE REGISTERED IN.**
- **PROVIDE YOUR ANSWERS IN THE SPACE PROVIDED ON THE QUESTION SHEET.**
- **THE SCRATCH BOOKLET WILL NOT BE CONSIDERED IN GRADING.**
- **BE AS NEAT AND CLEAR AS POSSIBLE.**

Problem	Total Points	Earned Points
1	12	
2	12	
3	12	
4	10	
5	12	
6	20	
7	10	
8	12	
Total	100	

Problem 1: AND-XOR Canonical Form [12 points]

Let $F(a, b)$ be a Boolean function of two variables. We know that F can be written as a canonical sum-of-product as follows:

$$F(a, b) = \bar{a} \cdot \bar{b} \cdot F(0,0) + \bar{a} \cdot b \cdot F(0,1) + a \cdot \bar{b} \cdot F(1,0) + a \cdot b \cdot F(1,1)$$

An alternative canonical form of writing F is using only AND and XOR functions. Show how to express F using only AND and XOR functions. **HINT: each of the above product terms is a min-term, what property do the min-terms have in common and how is that useful for XOR functions?**

Solution:

Since the above expression has terms which are mutually exclusive (minterms, '+' can be replaced by \oplus)

$$\Rightarrow F(a, b) = \bar{a} \cdot \bar{b} \cdot F(0,0) \oplus \bar{a} \cdot b \cdot F(0,1) \oplus a \cdot \bar{b} \cdot F(1,0) \oplus a \cdot b \cdot F(1,1)$$

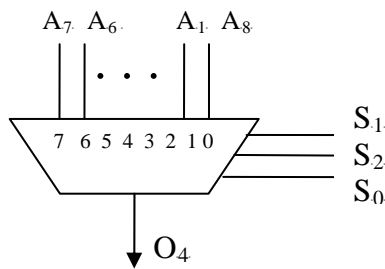
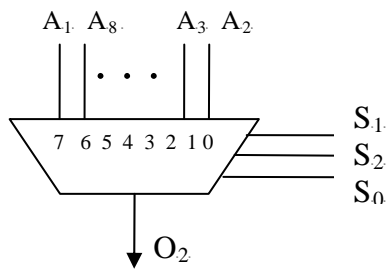
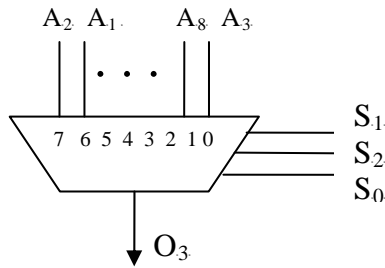
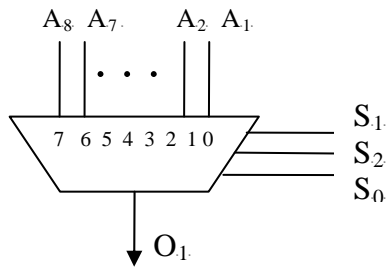
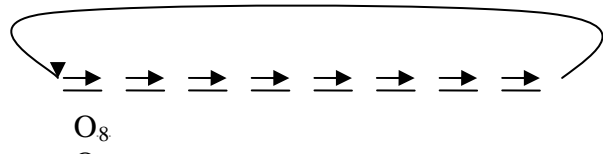
the inverted variables (e.g. \bar{a}) can be replaced with $a \oplus 1$

Problem 2: Combinational Shifter [12 points]

Design a combinational logic circuit with 8 data inputs A_1, A_2, \dots, A_8 , three control inputs S_2, S_1, S_0 , and 8 outputs O_1, O_2, \dots, O_8 . The output word is equal to the input word, rotated to the right circularly by a number of bit positions specified by the control inputs. For example, if the input word is 10111010 and the control inputs are 011, then the output word is 01010111. Label your inputs and outputs clearly.

Solution:

S2	S1	S0	
0	0	0	no rotation
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7



Problem 3: MN Flip Flop [12 points]

A *MN* flip-flop has two inputs *M* and *N*, and outputs *Q* and *Q'*. Input *M* behaves like the complement of the *J* input of a *JK* flip-flop, and input *N* behaves like the *K* input of a *JK* flip-flop.

(a) Obtain the characteristic equation of the *MN* flip-flop. [2 points]

M	N	Q Q*
0	0	1
0	1	last Q'
1	0	last Q
1	1	0

Q \ MN	00	01	10	11
0	1	1	1	1
1	1	1	1	1

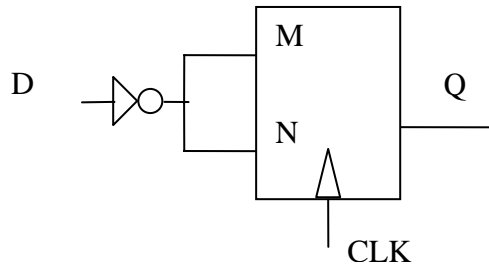
$M=J'$
 $N=K$
 $Q^*=Q'M' + QN'$

(b) Complete the following table for the *MN* flip-flop. You must specify the appropriate values to be applied on *M* and *N* to obtain the corresponding transition from *Q* to *Q**. [4 points]

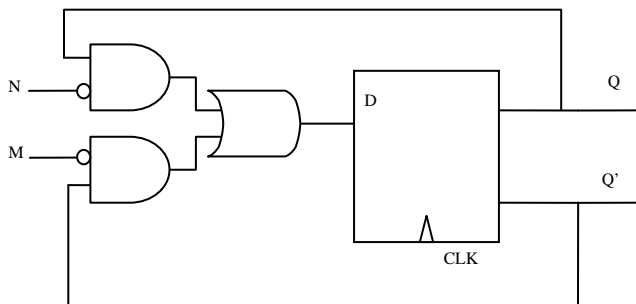
M	N	Q	Q*
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Current State	Next State	Inputs to be applied	
Q	Q*	M	N
0	0	1	d
0	1	0	d
1	0	d	1
1	1	d	0

(c) Design a *D* flip-flop using an *MN* flip-flop. [3 points]

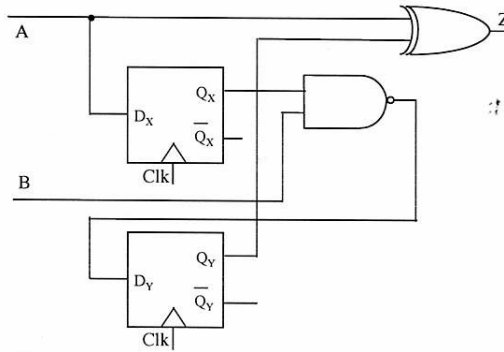


(d) Design an *MN* flip-flop using a *D* flip-flop. [3 points]



Problem 4: FSM Analysis [10 points]

Consider the following sequential circuit.



a) Is this a Mealy Machine or a Moore Machine? [1 point] Answer = *Mealy Machine*

b) Write Boolean equations for D_x , D_y , and Z . [3 points]

$D_x = A$, $D_y = \overline{Q_x} \cdot B$, $Z = A \oplus A_y$

c) Draw a state/Output table for the circuit. [3 points]

Q_x	Q_y	A	B	D_x	D_y	Z
0	0	0	0	0	1	0
0	0	0	1	0	1	0
0	0	1	0	1	1	1
0	0	1	1	1	1	1
0	1	0	0	0	1	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
0	1	1	1	1	1	0
1	0	0	0	0	1	0
1	0	0	1	0	0	0
1	0	1	0	1	1	1
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	0	0	1
1	1	1	0	1	1	0
1	1	1	1	1	0	0

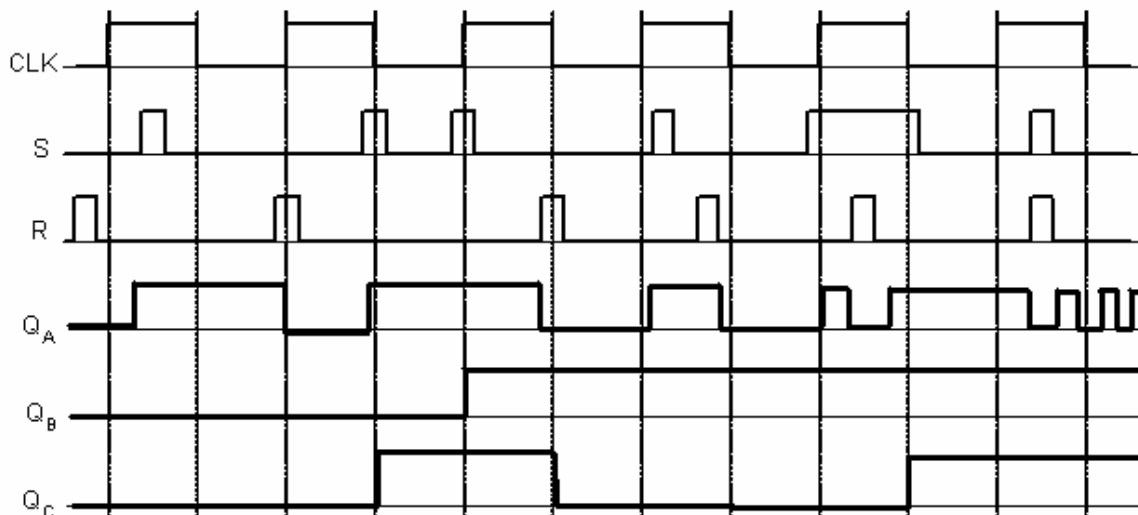
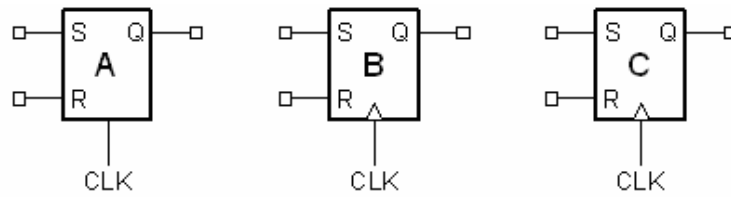
d) Draw the corresponding state diagram. [3 points]

Problem 5: Latches versus Flip Flops [12 points]

Device A shown below is a level sensitive SR latch (i.e., it reacts to the S, R inputs when the clock is high). Device B is an SR flip flop that is positive edge triggered. Device C is an SR flip flop that is negative edge triggered.

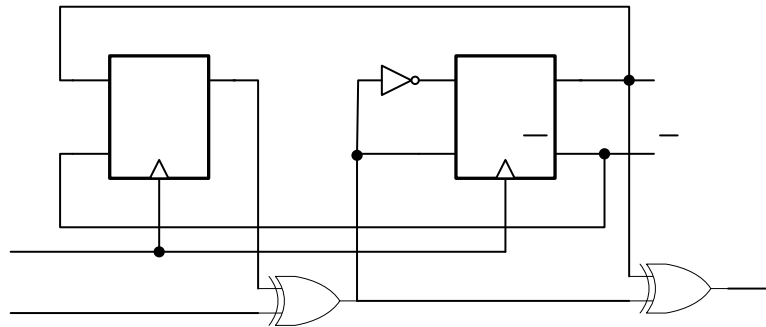
Assume 0 setup and hold times, and 0 propagation delays. All devices treat R and S as active high signals (i.e., reset when R is true, and Set when S is true), and are implemented using NOR gates. Initially the devices have 0 stored in them.

Complete the timing diagram below for the signals Q_A , Q_B , and Q_C , showing the behavior of the three different devices to the same S and R input changes.



Problem 6: FSM Analysis and Design [20 points]

The sequential circuit shown below has one input X, one output Y, and is implemented using two SR flip flops.



a) Derive the state/output table of the circuit. [4 points]

Solution:

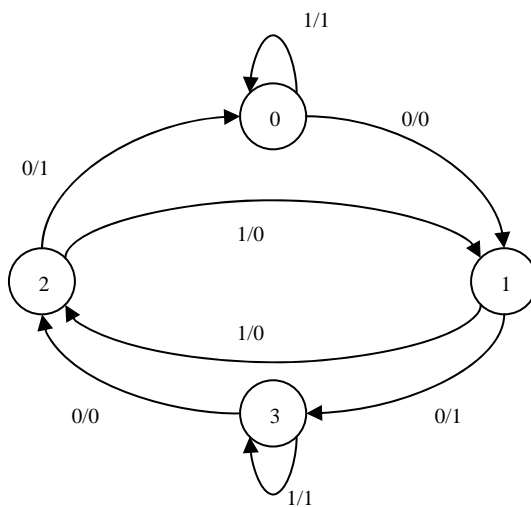
$$S_A = B$$

$$R_A = \overline{B}$$

$$S_B = \overline{X \oplus A}$$

$$R_B = X \oplus A$$

Present state		Input	Next state		Output
A	B	X	A	B	Y
0	0	0	0	1	0
0	0	1	0	0	1
0	1	0	1	1	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	1	0	1	0
1	1	0	1	0	0
1	1	1	1	1	1

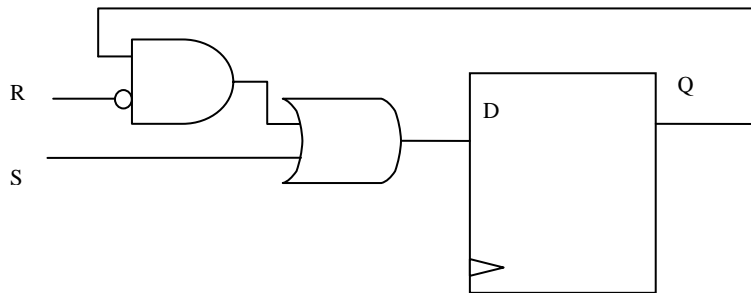


CLK

X

b) Redesign the above circuit using D flip flops instead of SR flip flops. [8 points]

Solution:



Q \ SR	00	01	11	10
0	0	0	d	1
1	1	0	d	1

c) Redesign the above circuit using JK flip flops instead of SR flip flops. [8 points]

Solution:

JUST

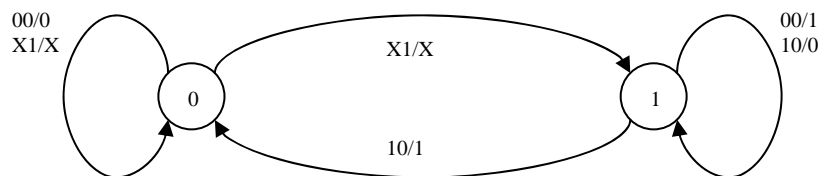
REPLACE

Problem 7: Serial 2's Complementer [10 points]

A serial two's complementer is to be designed. A binary integer of arbitrary length is presented to the serial two's complementer, least significant bit first, on input X. When a given bit is presented on input X, the corresponding output bit is to appear during the same clock cycle on output Z. To indicate that a sequence is complete and that the circuit is to be initialized to receive another sequence, input Y becomes 1 for one clock cycle. Otherwise, Y is 0. Draw the state diagram for the two's complementer circuit. Identify the meaning of each state in your diagram.

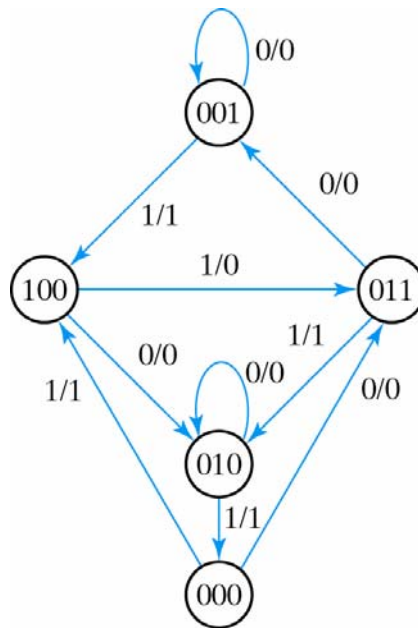
Solution:

Present state	Inputs		Next state	Output
Q(t)	X	Y	Q(t+1)	Z
0	0	0	0	0
0	0	1	0	X
0	1	0	1	1
0	1	1	0	X
1	0	0	1	1
1	0	1	0	X
1	1	0	1	0
1	1	1	0	X



Problem 8: FSM Design [12 points]

A sequential circuit has three flip flops A, B, C; one input x; one output y. The state diagram is shown below. The circuit is to be designed by treating the unused states as don't cares. Design the FSM using D flip flops.



Solution:

			X	
Q ₂	Q ₁	Q ₀	0	1
0	0	0	011/0	100/1
0	0	1	001/0	100/1
0	1	0	010/0	000/1
0	1	1	001/0	010/1
1	0	0	010/0	011/0
1	1	1	D	D
1	1	0	D	D
1	0	1	D	D

Q ₁ , Q ₀		00	01	11	10
D ₂	00	0	0		1
	01		d	d	1
	11		d	d	
	10		d	d	

$D_2 = X'Q_1Q_0$

		Q_1, Q_0			
		00	01	11	10
XQ_2	00	1	1	1	
	01		d	d	
	11		d	d	1
	10	1	d	d	

$$D1 = Q_0 + Q_2'Q_1' + XQ_2Q_1$$

		Q_1, Q_0			
		00	01	11	10
XQ_2	00	1	1	1	
	01		d	d	
	11		d	d	1
	10	1	d	d	

$$D_0 = Q_2Q_1' + X'Q_1'Q_0' + Q_1Q_0$$